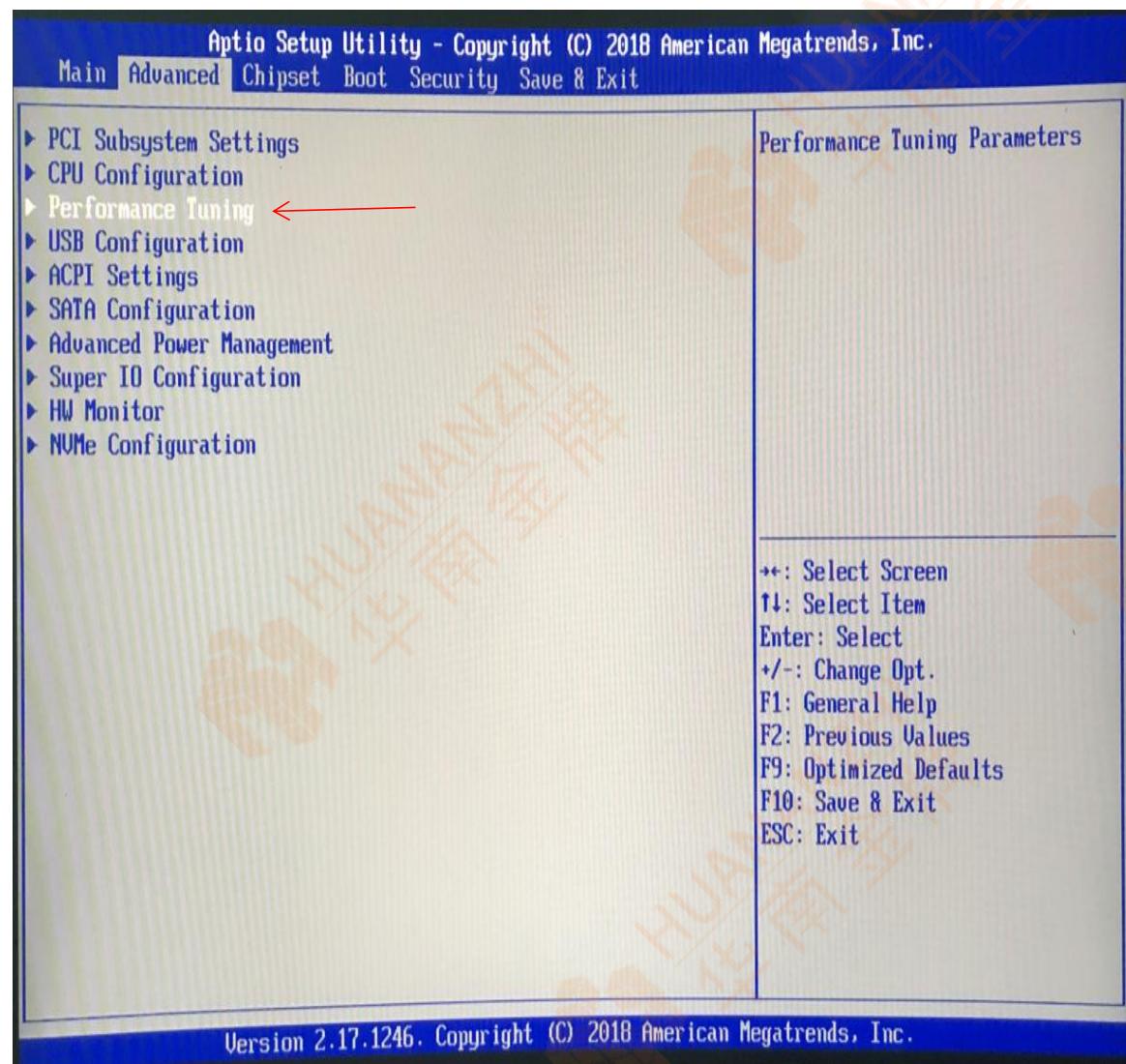
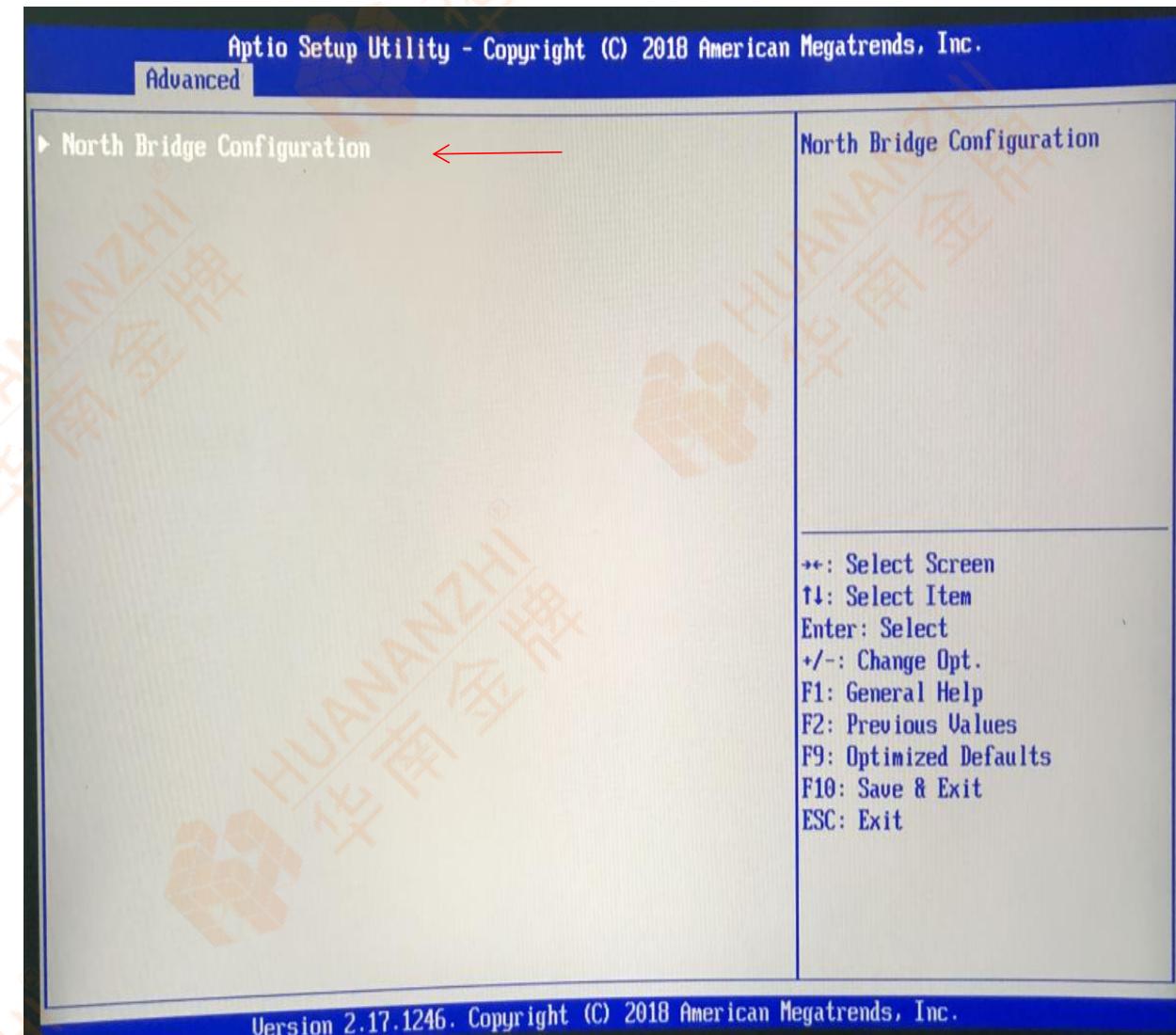


内存频率设置

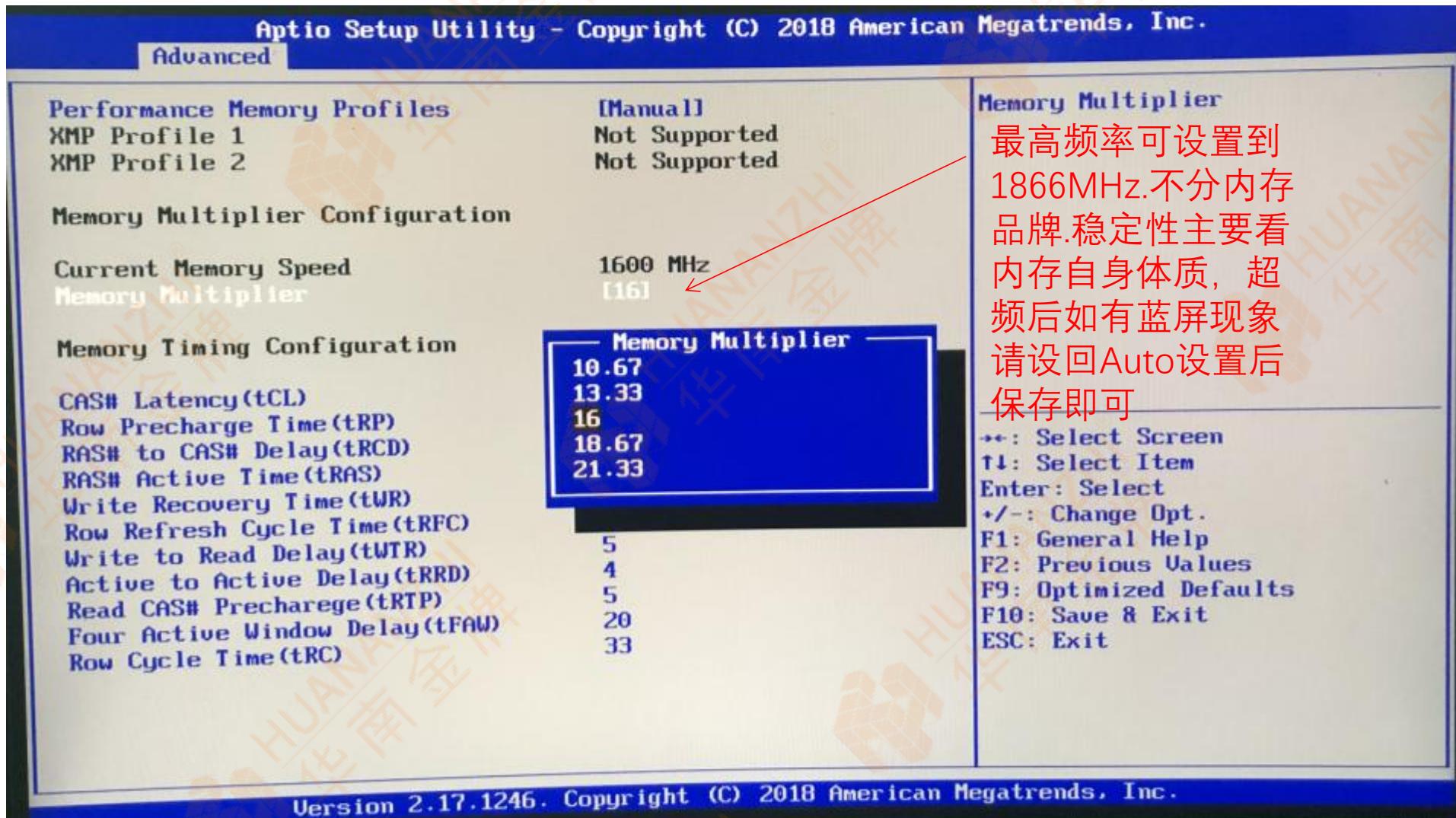
第一步



第二步

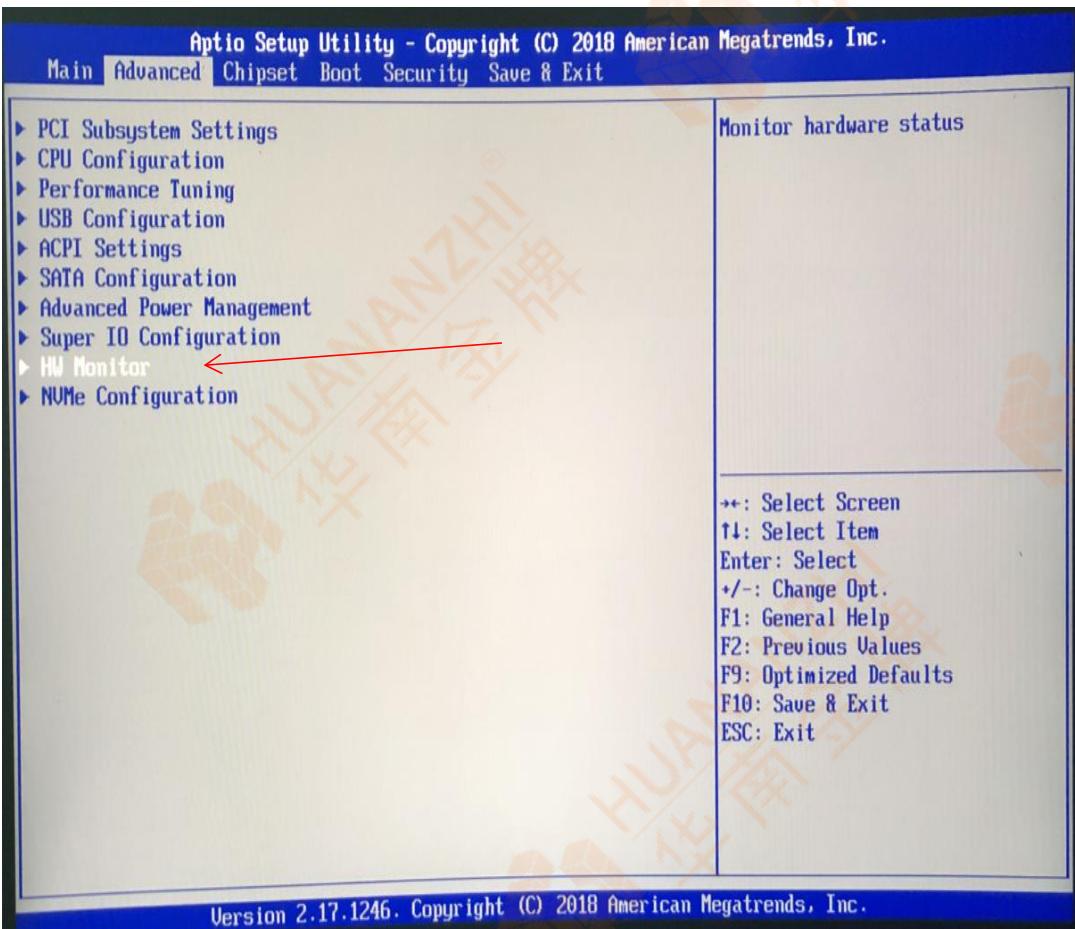


第三步

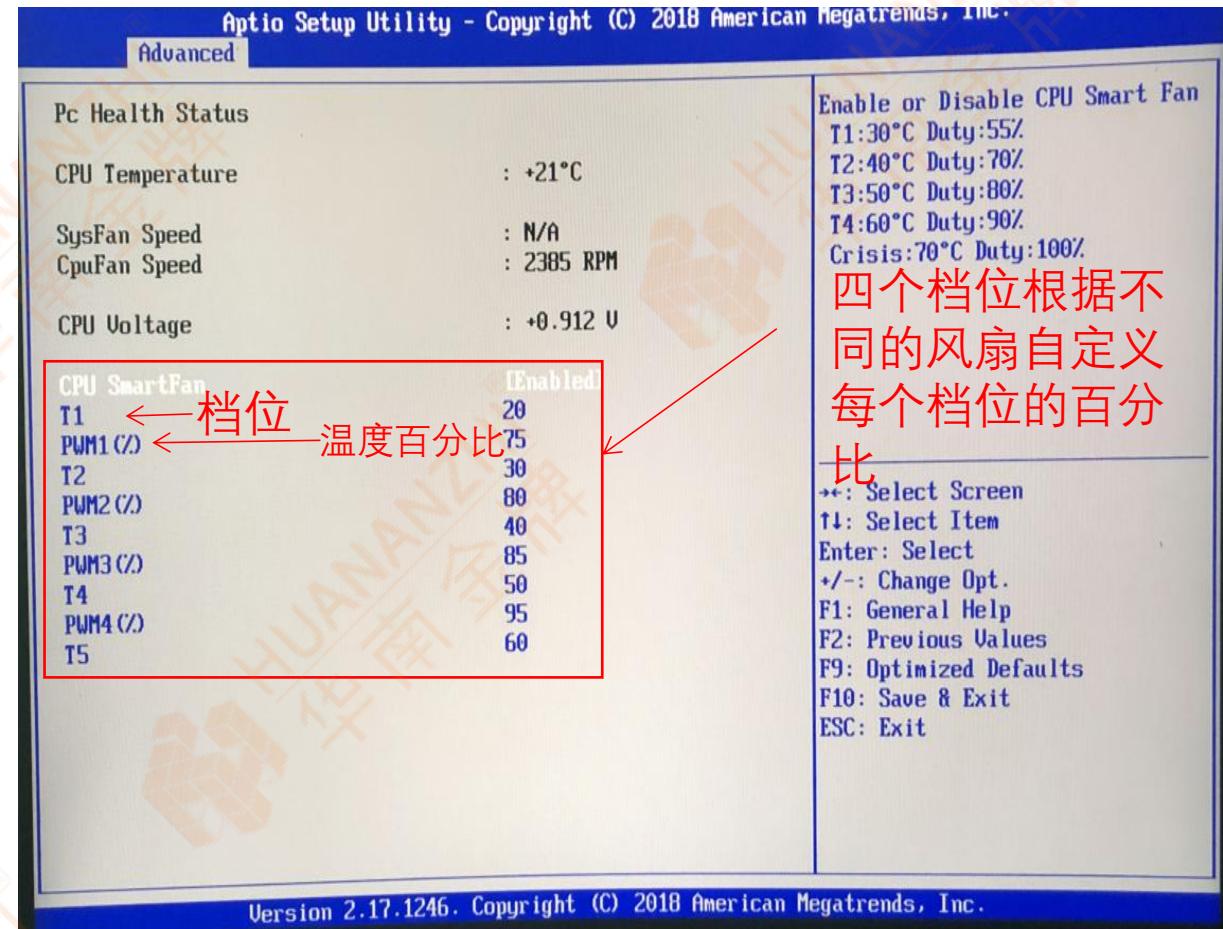


风扇调速设置

第一步

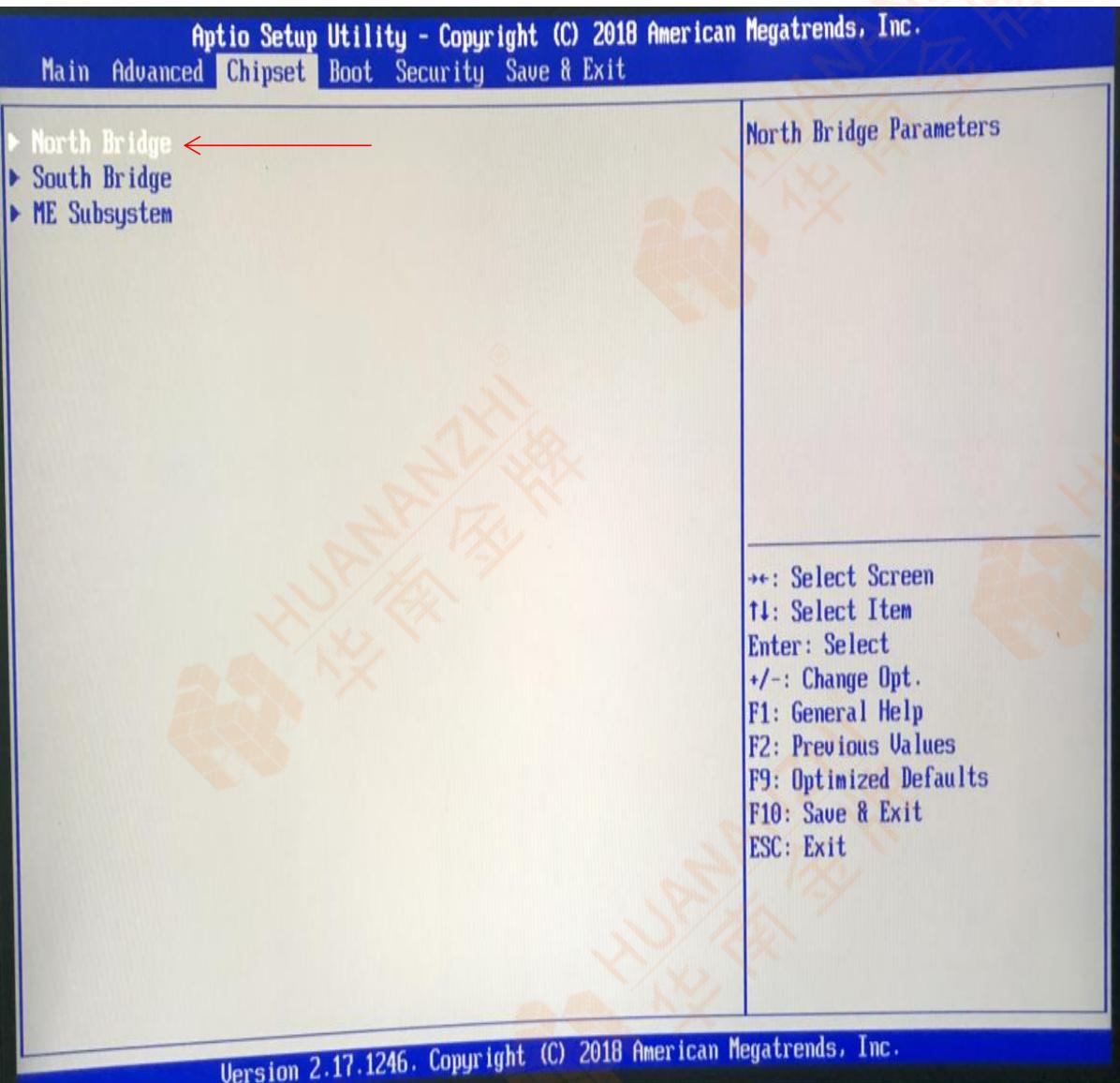


第二步

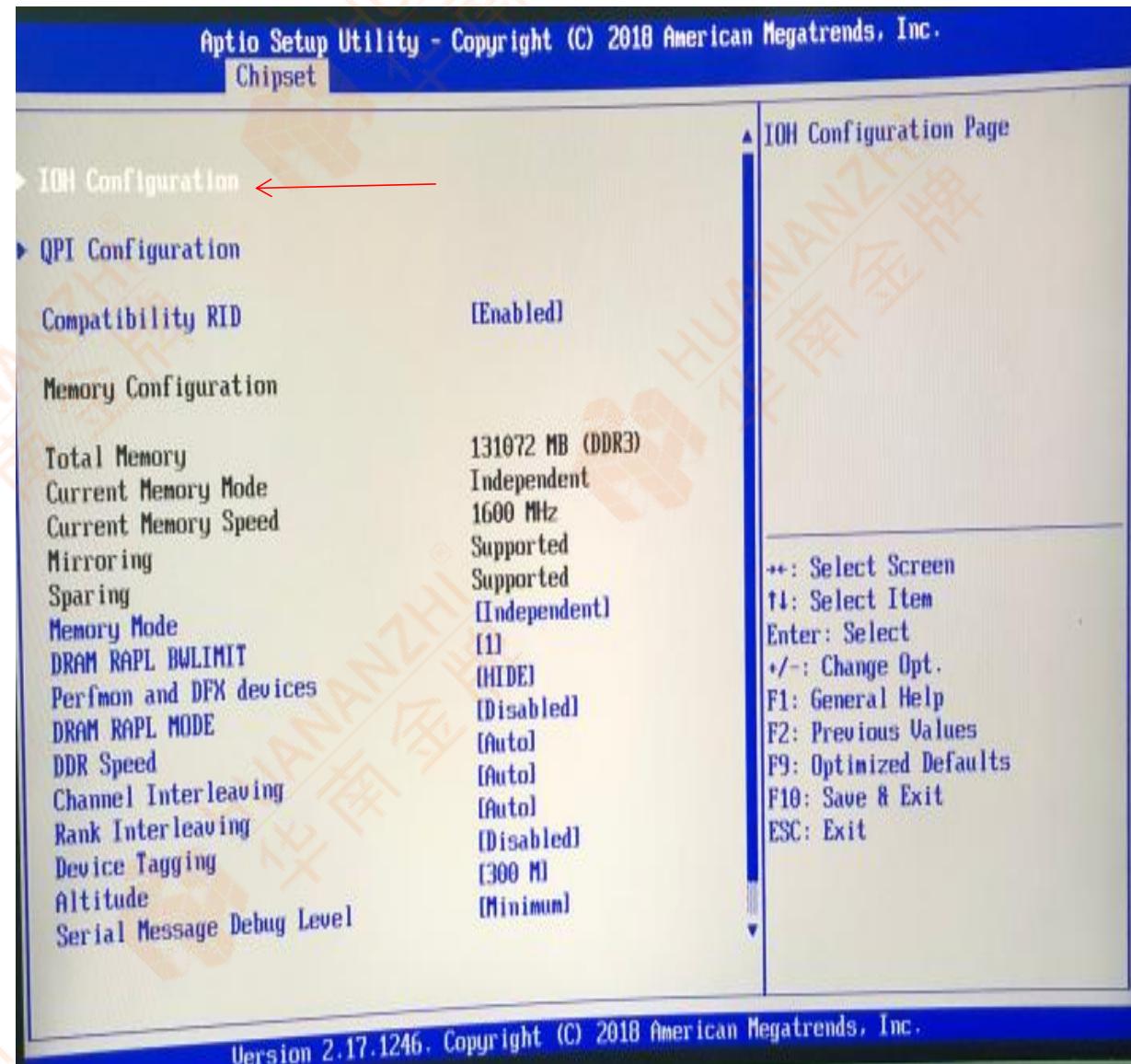


VT-D虚拟化开启设置

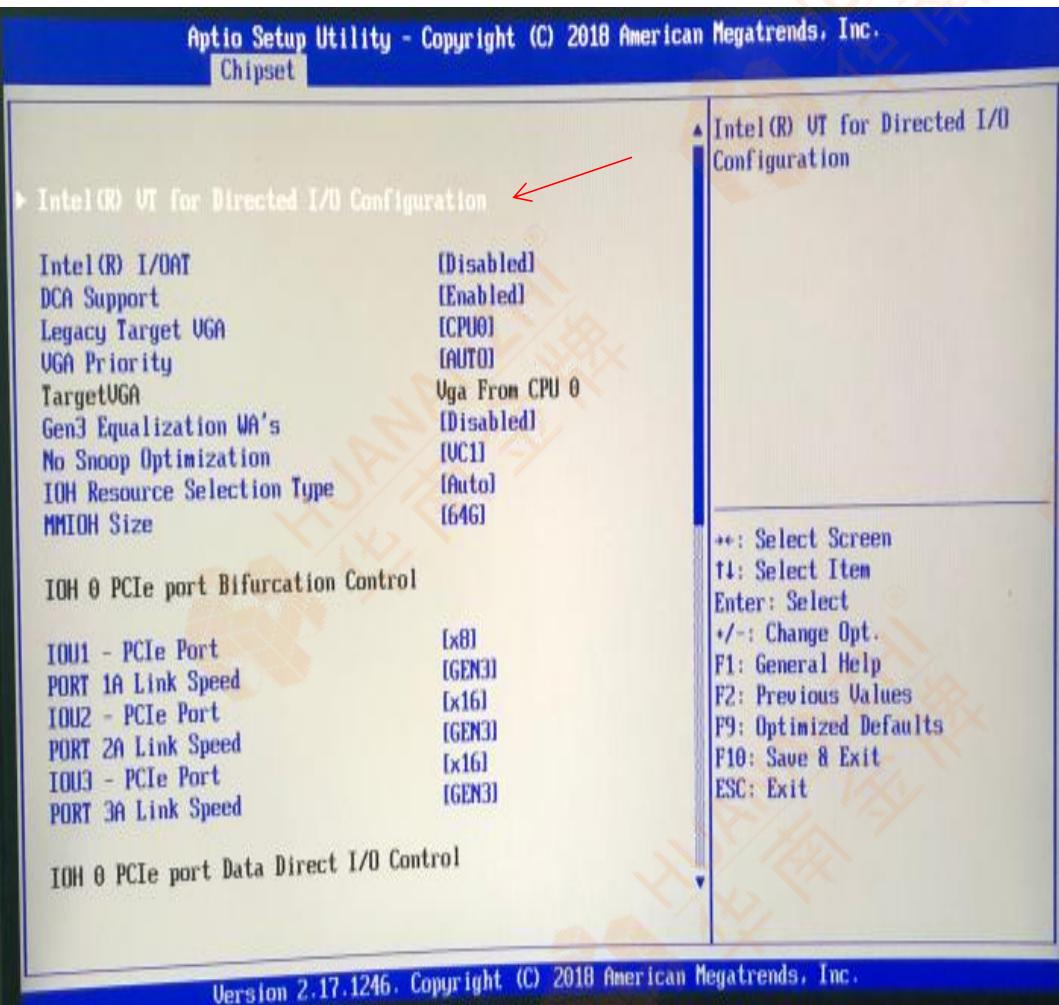
第一步



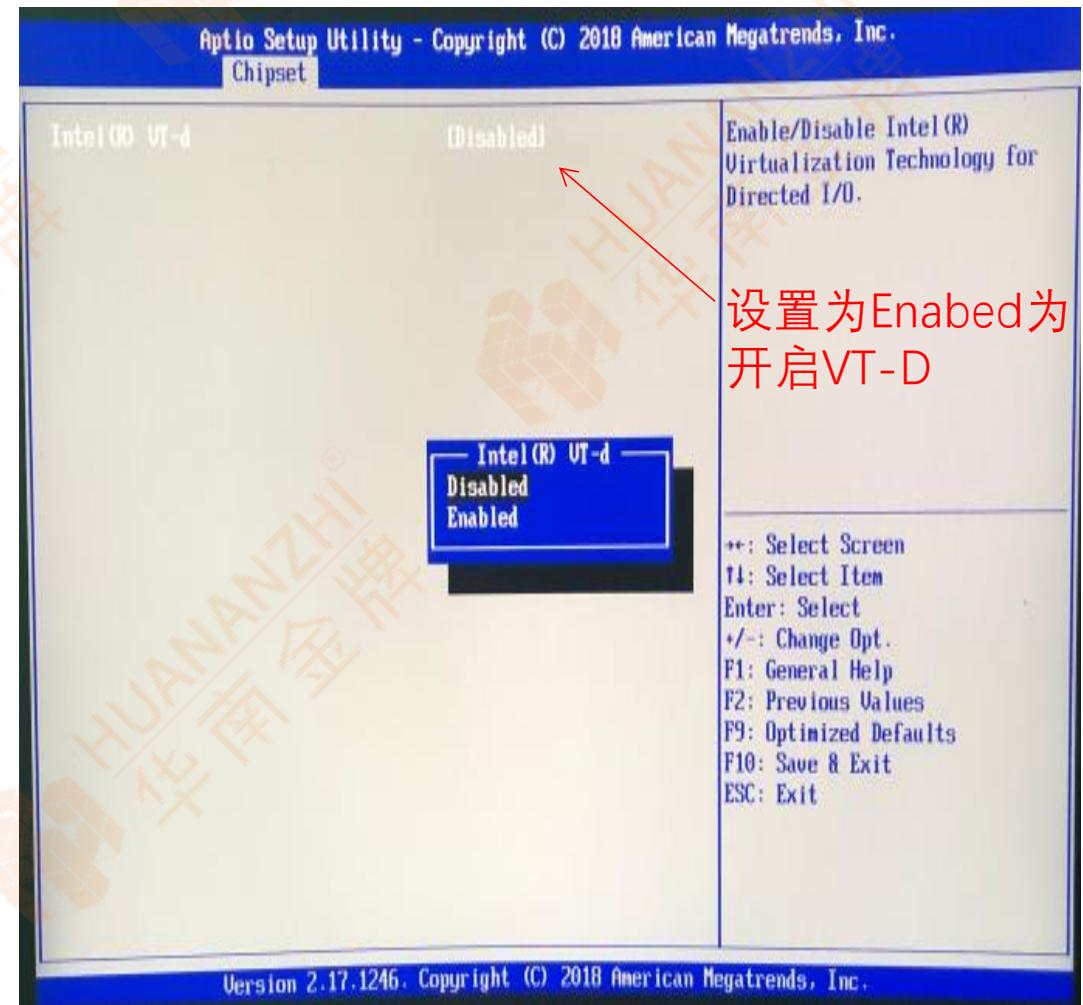
第二步



第三步

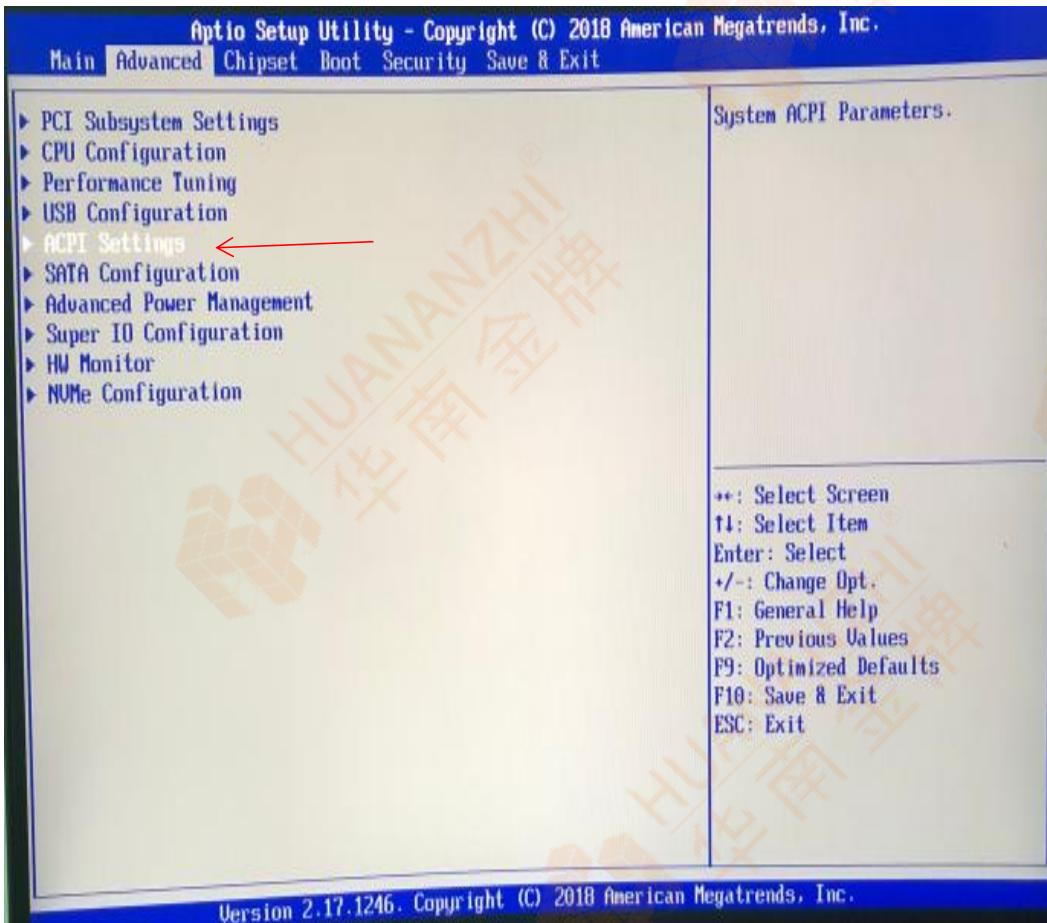


第四步

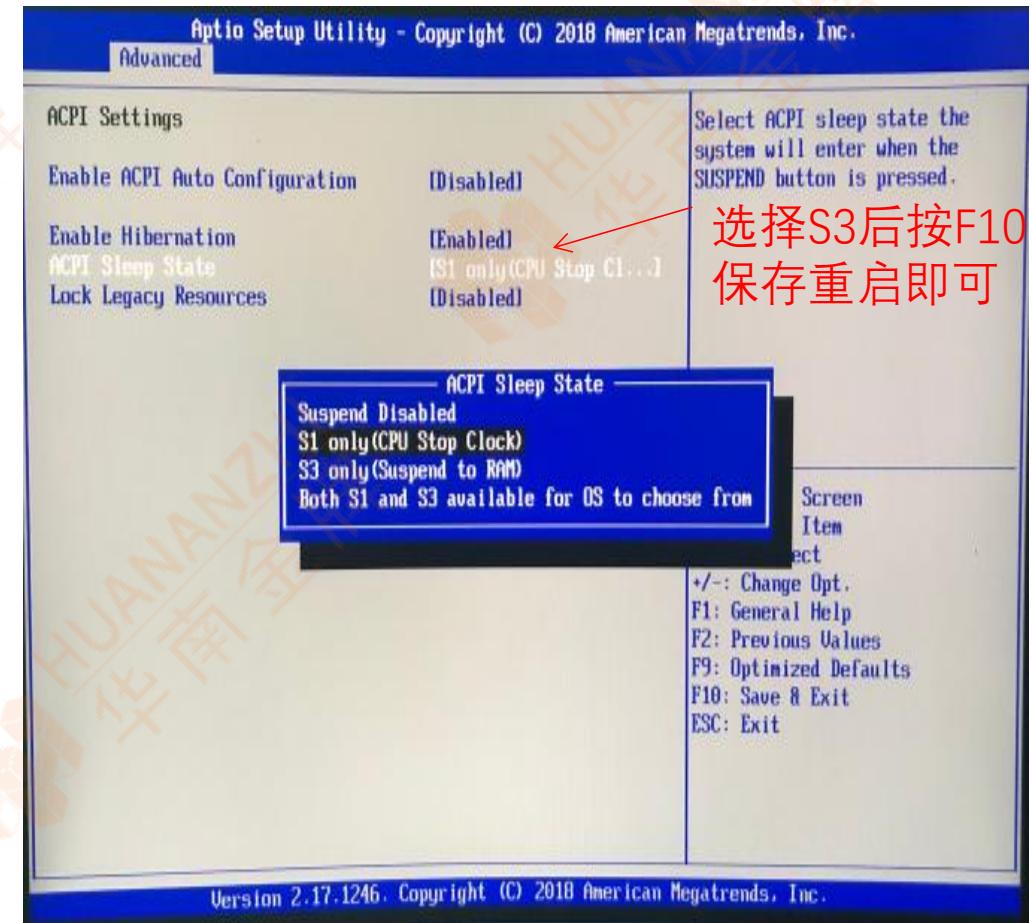


S3睡眠模式设置

第一步

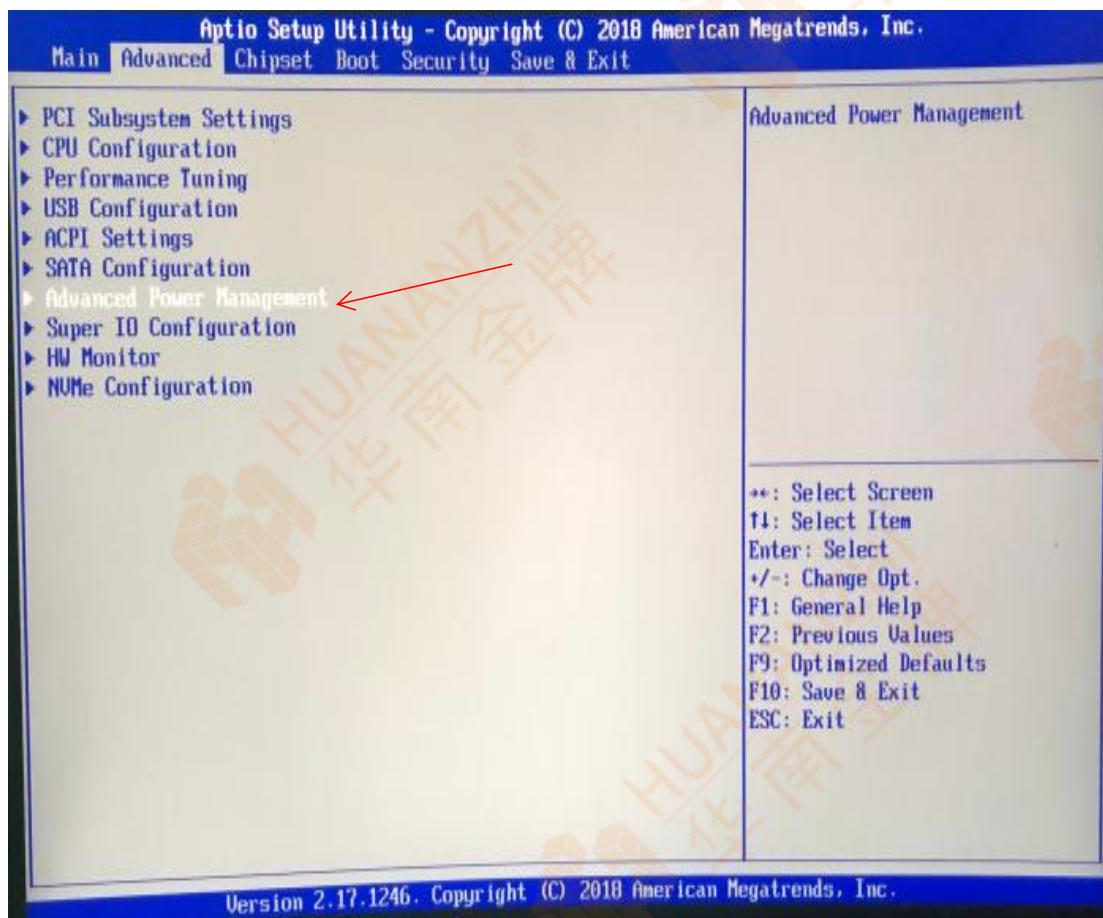


第二步



AC启动/网络唤醒设置

第一步

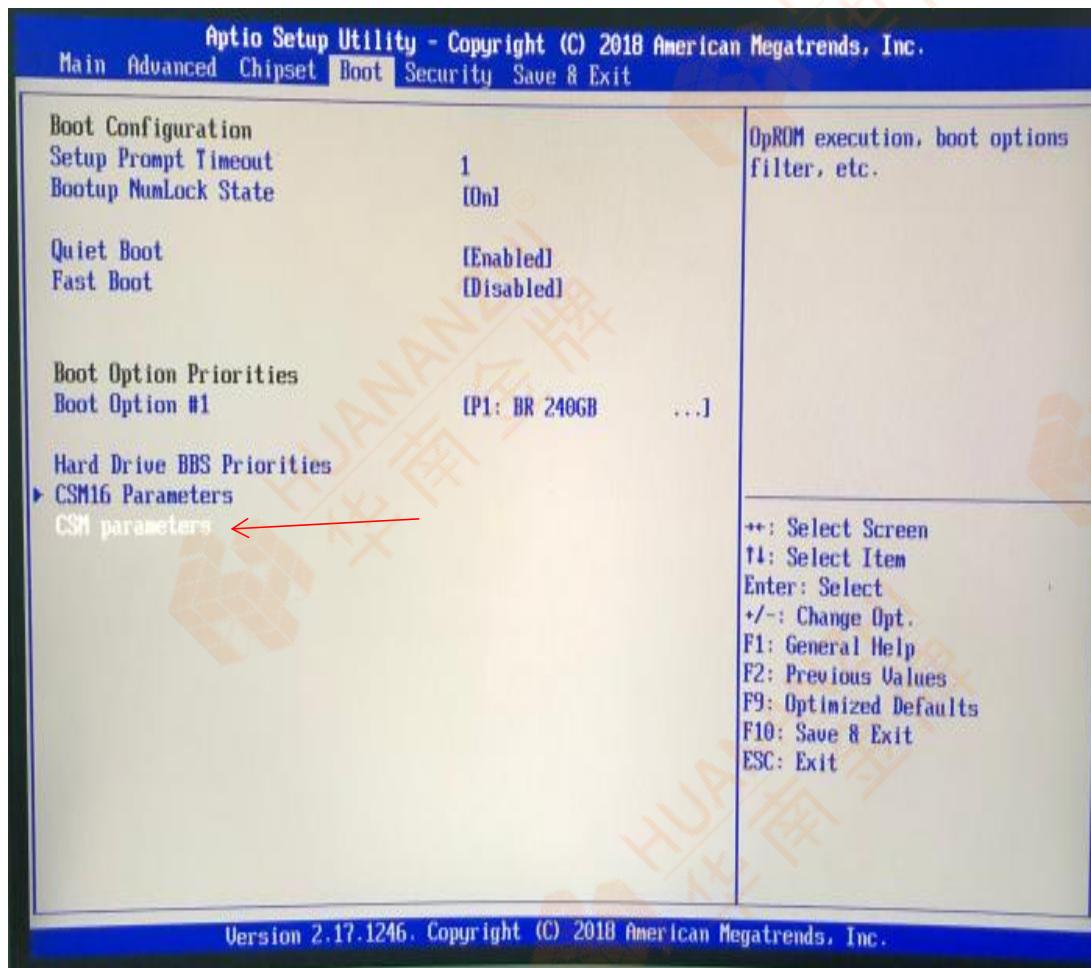


第二步

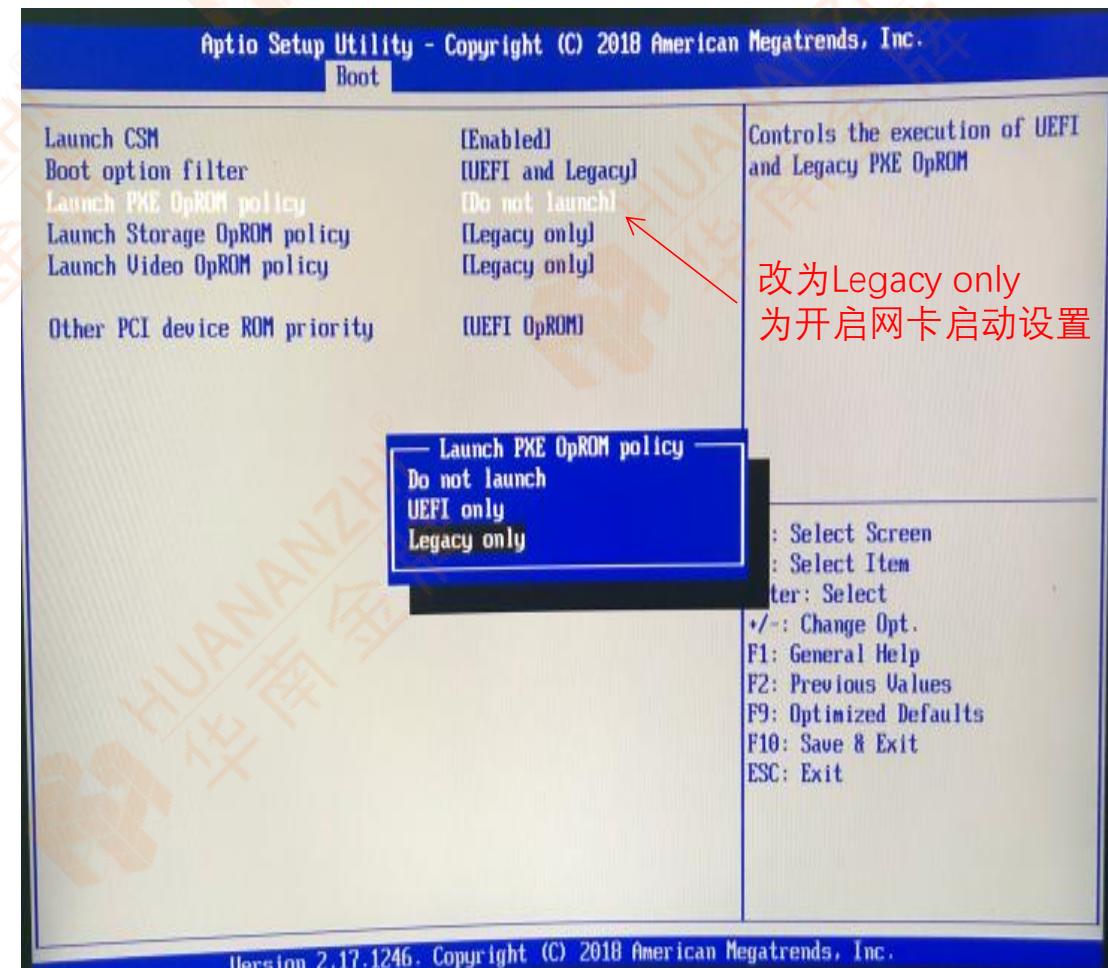


网卡启动设置

第一步

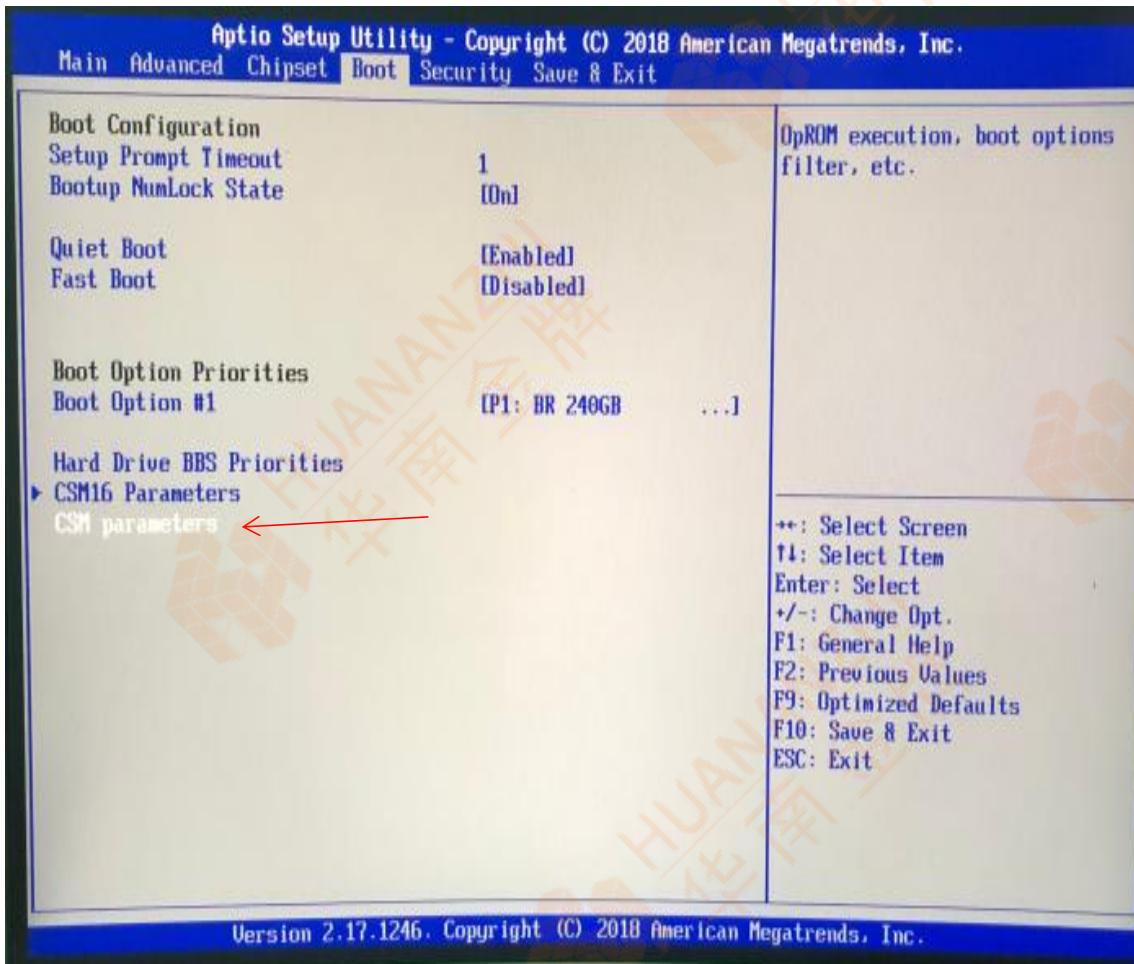


第二步

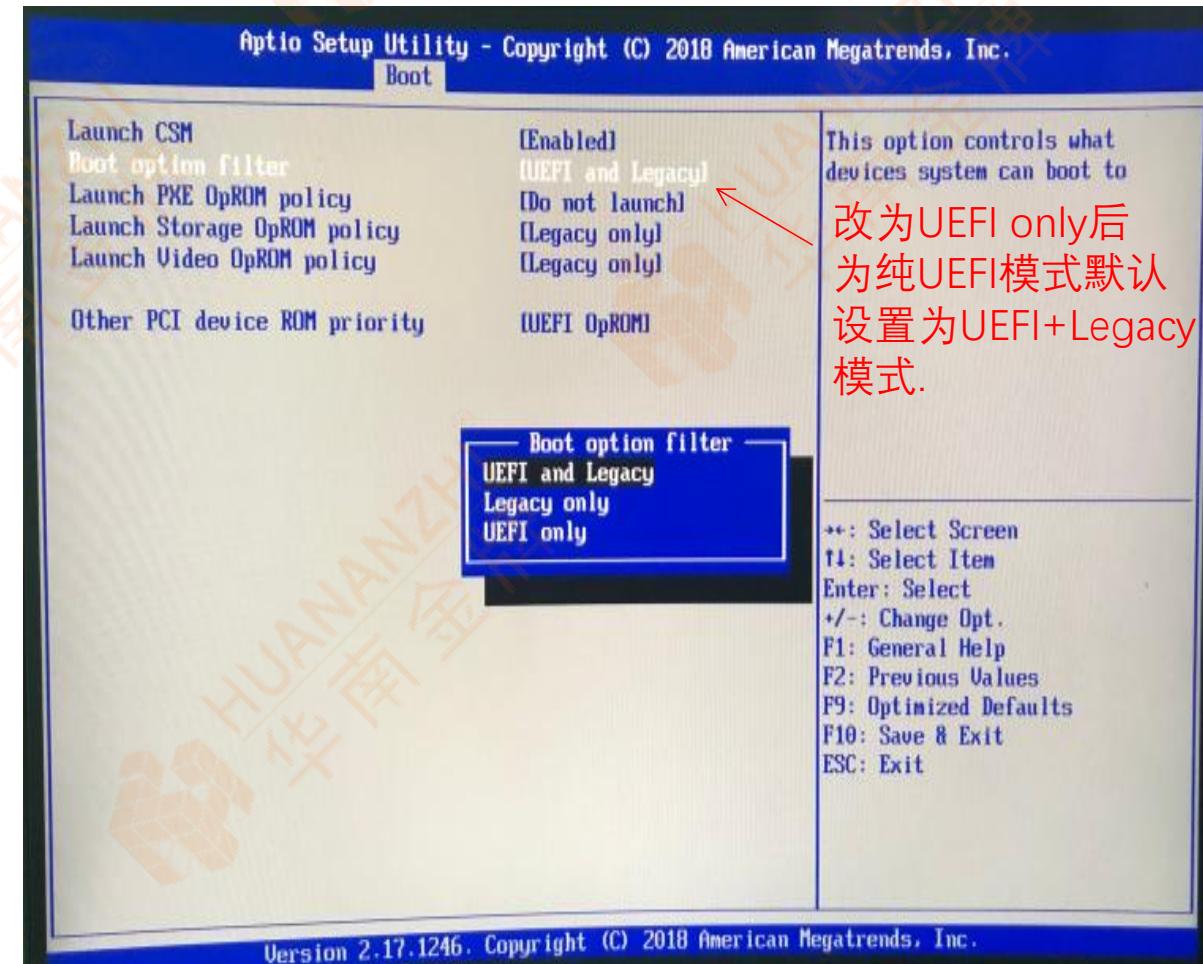


纯UEFI模式设置

第一步



第二步



PCIE 拆分教程

Aptio Setup Utility - Copyright (C) 2019 American Megatrends, Inc.

Main Advanced Chipset Boot Security Save & Exit

- ▶ North Bridge
- ▶ South Bridge
- ▶ ME Subsystem

第一步

North Bridge Parameters

**: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F9: Optimized Defaults
F10: Save & Exit
ESC: Exit

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PCIe Setup Utility - Copyright (C) 2019 American Megatrends, Inc.

Chipset

▶ IOH Configuration

▶ QPI Configuration

Compatibility RID

Memory Configuration

Total Memory

Current Memory Mode

Current Memory Speed

Mirroring

Sparing

Memory Mode

DRAM RAPL BWLIMIT

Perfmon and DFX devices

DRAM RAPL MODE

DDR Speed

Channel Interleaving

Rank Interleaving

Device Tagging

Altitude

Serial Message Debug Level

[Enabled]

第二步

16384 MB (DDR3)

Independent

1333 MHz

Supported

Not Possible

[Independent]

[1]

[HIDE]

[Disabled]

[Auto]

[Auto]

[Auto]

[Disabled]

[300 M]

[Minimum]

**: Select Screen

↑↓: Select Item

Enter: Select

+/-: Change Opt.

F1: General Help

F2: Previous Values

F9: Optimized Defaults

F10: Save & Exit

ESC: Exit

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PCIE 拆分教程

LED19W

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Chipset

► Intel(R) VT for Directed I/O Configuration

Intel(R) I/OAT	[Disabled]
DCA Support	[Enabled]
Legacy Target VGA	[CPU0]
VGA Priority	[AUTO]
TargetVGA	Vga From CPU 0
Gen3 Equalization WA's	[Disabled]
No Snoop Optimization	[VC1]
IOH Resource Selection Type	[Auto]
MMIOH Size	[64G]

IOH 0 PCIe port Bifurcation Control

IOU1 - PCIe Port	[x4x4]
PORT 1A Link Speed	[GEN3]
PORT 1B Link Speed	[GEN3]
IOU2 - PCIe Port	[x16]
PORT 2A Link Speed	[GEN3]
IOU3 - PCIe Port	[x16]
PORT 3A Link Speed	[GEN3]

IOH 0 PCIe port Data Direct I/O Control

▲ Functions visible based on this setting : x4x4 (Fun 0/1 visible) x8 (Fun 1 visible)

++: Select Screen
†: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F9: Optimized Defaults
F10: Save & Exit
ESC: Exit

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Chipset

► Intel(R) VT for Directed I/O Configuration

Intel(R) I/OAT	[Disabled]
DCA Support	[Enabled]
VGA Priority	[Offboard]
TargetVGA	Vga From CPU 0
Gen3 Equalization WA's	[Enabled]
Gen3 Equalization Fail WA	[Disabled]
Gen3 Equalization Phase 2/3 WA	[Disabled]
Gen3 Equalization Redoing WA	[Disabled]
IOH Resource Selection Type	No Snoop Optimization
MMIOH Size	MMCQ BASE

IOH 0 PCIe port Bifurcation Control

IOU1 - PCIe Port	[x4x4]
PORT 1A Link Speed	[GEN3]
PORT 1B Link Speed	[GEN3]
IOU2 - PCIe Port	[x16]
PORT 2A Link Speed	[GEN3]
IOU3 - PCIe Port	[x16]
PORT 3A Link Speed	[GEN3]

IOU2 - PCIe Port	x4x4x4x4
	x4x4x8
	x8x4x4
	x8x8
	x16

▲ Functions visible based on this setting : x4x4x4x4 (Fun 0/1/2/3 visible) x4x4x8 (Fun 0/2/3 visible) x8x4x4 (Fun 0/1/2 visible) x8x8 (Fun 0/2 visible) x16 (Fun 0 Visible)

++: Select Screen
†: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

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